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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,762	06/30/2003	Karl H. Mauritz	884.925US1	5893

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EXAMINER	
JOSEPH, JAISON	
ART UNIT	PAPER NUMBER
2611	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/612,762	MAURITZ ET AL.	
	Examiner	Art Unit	
	Jaison Joseph	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) *30-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,21-29 and 33-35* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

35 USC § 112 rejection of claim 27 is withdrawn.

Applicant's arguments with respect to claims 1 – 35 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 4, 8, 12, 13, 21 – 24, 26, 28, and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Tabatabaei (US Patent 6,784,740).

Regarding claim 1, Tabatabaei teaches an article comprising: a first peak detector to generate an output in response to detection of a peak amplitude of a received signal at an input terminal (see figure 3, component 335 see input signal coming into the peak detector 335 and the output signal going to the amplifier 350); a first amplifier to compare the peak amplitude and a first reference potential and generate a feedback signal coupled through a resistance to the input terminal (see figure 3, component 350, output received from the peak detector 335, and comparing the said output signal with reference input from the component 345 and generating the

feedback signal couple through a resistance 355 to the input terminal 315) ; and a second amplifier to compare the received signal and a second reference potential (see figure 3, component 300, 305, 310, 320, 325 and see the inputs to 310 and 305, output signal *out* is determined by the comparison of gate potentials at transistors 305 and 310).

Regarding claim 3, which inherits the limitations of claim 1, Tabatabaei further teaches further including a capacitor coupled to the input terminal to provide isolation (see figure 4, component 404).

Regarding claim 4, which inherits the limitations of claim 1, Tabatabaei further teaches wherein the first peak detector includes a maximum high-level peak detector (see figure 3, component 335).

Regarding claim 8 Tabatabaei teaches a circuit comprising: a feedback amplifier (see figure 3, component 350) having a feedback output (output of component 350) and a first feedback input (input signal received from component 335) and having a second feedback input to couple with a first reference potential (see figure 3, input received from component 345); a peak detector (figure 3, component 335) having a detector output coupled to the first feedback input (see figure 3, output of 335 is coupled to component 350) and having a detector input (see figure 3, input to component 335); a feedback circuit coupled to the feedback output and coupled to the detector input (see figure 3, component 355 and node 315); and a receiver amplifier having a first receiver input coupled to the detector input and having a second receiver input adapted to couple with a second reference potential (see figure 3, component 300, 305, 310, 320,

325 and see the inputs to 310 and 305, output signal *out* is determined by the comparison of gate potentials at transistors 305 and 310).

Regarding claim 12, Tabatabaei teaches a system comprising: a driver having a primary output terminal (see figure 4, the RF signal); a receiver having a primary input terminal coupled to the primary output terminal (see figure 4, RF in signal); a primary peak detector coupled to the primary input terminal and having a primary peak an output amplifier having a first amplifier input coupled to the primary input terminal and a second amplifier input coupled to a first reference potential (see component 400); a primary feedback amplifier having a first primary feedback input coupled to the primary peak output and a second primary feedback input coupled to a second reference potential and having a primary feedback output (see figure 4, component 422); and a primary feedback circuit coupled to the primary feedback output and coupled to the primary input terminal (see figure 4, component 432).

Regarding claim 13, which inherits the limitations of claim 12, Tabatabaei further teaches further including a capacitor between the primary output terminal and the primary input terminal (see figure 4, component 404).

Regarding claim 21, Tabatabaei teaches a method comprising: detecting a peak amplitude of an input signal (see figure 3, component 335); generating a feedback signal as a function of a comparison of the peak amplitude and a first reference potential (see figure 3, component 335, 350, 355, 315); biasing the input signal with the feedback signal 9see figure 3, component 330); and generating an output signal as a function of a comparison of the input signal and a second reference potential (see figure

3, component 3, the output signal and component 300, 305, 310, 320, 325 and see the inputs to 310 and 305, output signal *out* is determined by the comparison of gate potentials at transistors 305 and 310).

Regarding claim 22, which inherits the limitations of claim 21, Tabatabaei further teaches wherein detecting the peak includes detecting a peak high value (see figure 3, and column 2, lines 52 – column 4, lines 3).

Regarding claim 23, which inherits the limitations of claim 21, Tabatabaei further teaches wherein generating the feedback signal includes generating an amplified signal based on a differential between the peak and the first reference level (see figure 3, and column 2, lines 52 – column 4, lines 3).

Regarding claim 24, which inherits the limitations of claim 21, Tabatabaei further teaches wherein detecting the peak in the input signal includes receiving the input signal from a signal source and further including receiving the second reference potential from the signal source (see figure 3, and column 2, lines 52 – column 4, lines 3).

Regarding claim 26, Tabatabaei teaches a method comprising: receiving a first reference potential (see figure 3, input signal); sampling an input signal relative to the first reference potential (see figure 3, component 350); generating a correction signal based on a peak amplitude in the sampled input signal (see figure 3, component 330); and biasing the input signal as a function of the correction signal (see figure 3, component 330 and column 2, lines 52 – column 4, lines 3).

Regarding claim 28, which inherits the limitations of claim 26, Tabatanaei further teaches wherein generating the correction signal based on the peak amplitude in the sampled input signal includes detecting the maximum high value in the sampled input signal (see figure 3, and column 2, lines 52 – column 4, lines 3).

Regarding claim 29, which inherits the limitations of claim 26, Tabatabaei further teaches wherein biasing includes generating a differential amplified signal based on a comparison of the peak amplitude and a second reference potential (see figure 3, and column 2, lines 52 – column 4, lines 3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 11, 14, 15, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tabatabaei (US Patent 6,784,740).

Regarding claim 7, 11, and 14, Tabatabaei further teaches inludign a flter coupled to the amplifier (see figure 3, component 355 and figure 4, component 432 and column 3, lines 56 – 65). Tabatabaei further teaches component 355 is coupled to the first amplifier and is used to allow only low frequency or DC component to pass through (see column 3, lines 56 – 65), which is functional equivalent to a low pass filter.

Therefore it would be obvious to an ordinary skilled in the art at the time the invention was made to use a RF choke to limit the bandwidth.

Regarding claim 15, which inherits the limitations of claim 14, Tabatabaei disclose the claimed invention except for having the filter includes a capacitor. It would have been obvious to an ordinary skilled in art at the time the invention was made to have a filter with a capacitor since it was known in the art that using capacitors as filters since capacitor filters are inexpensive and simple to design.

Regarding claim 18 and 19, which inherits the limitations of claim 12,Tabatabaei does not expressly teach the input terminal is coupled to output terminal by a cable or by a backplane. At the time the invention was made, it would have been obvious to a person if ordinary skilled in the art to have system provide having an input terminal coupled to output terminal by a cable or backplane. Applicant has not disclosed that coupling input terminal with output terminal by a cable or backplane provides an advantage, is used for a particular purpose, or solves a stated problem. Therefore it would have been obvious to one of ordinary skilled in the art to modify Tabatabaei to obtain the invention as specified in claims 18 and 19.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tabatabaei (US Patent 6,784,740) in view of Buchanan et al. (US Patent 4,550,342).

Regarding claim 5, which inherits the limitations of claim 1, Tabatabaei dies not expressly teach the first peak detector includes a minimum level peak detector. However, Buchanan et al teach a DC offset correction circuit having a negative peak detector (see figure 2, and column 3, lines 9 – column 4, line 25). Therefore it would be

obvious to an ordinary skilled in the art at the time the invention was made to use a negative peak detector in place of the Tabatabaei's peak detector. The motivation or suggestion to do so is that the negative peak detector does not tend to saturate and does not require a reset function to prevent saturation.

Claims 6, 9, 10, 16, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tabatabaei (US Patent 6,784,740) in view of Takahashi et al (USPAP 2003/0128558).

Regarding claim 6, 9, 10, 16 and 17 Tabatabaei does not expressly teach resistance includes a transistor. However it is well known in the art to use a transistor for resistance. Further Tabatabaei further teaches the component 355 can be realized by using other devices. And further Takahashi et al teach functions of inductors and resistors can be realized by using transistors. Therefore it would be obvious an ordinary skilled in the art at the time the invention was made to use a transistor for resistance. The motivation or suggestion to do so is to incorporate the circuit in a single substrate.

Claims 2, 25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tabatabaei (US Patent 6,784,740) in view of Khorram et al (US 2004/0190650) and further in view of Karsh et al (US Patent 4,641,324).

Regarding claim 2, which inherits the limitations of claim 1, Tabatabaei is cited as explained in the above paragraph. Tabatabaei does not expressly teach having a maximum level detector, minimum level detector, and a voltage divider to provide the second reference signal. However Khorran et al teach a maximum level detector, and a minimum level detector, each having an output coupled by a circuit to provide a

reference potential (see figure 8, components 104, 106, 108, 111). Khorram et al uses summing and scaling means to generate the reference potential of the voltage divider, such a difference is a matter of design choice. The usage of voltage divider to generate reference potential is well known in the art as shown in the Karsh et al. Therefore it would have been obvious to one ordinary skilled in the art at the time the invention was made to generate a reference potential through max and min peak values of the input signal in order to provide a most appropriate reference point for DC offset compensation.

Regarding claim 25, which inherits the limitations of claim 21, the claimed method including the features that correspond to subject matter mentioned above in the rejection of claim 2 is applicable hereto.

Regarding claim 27, which inherits the limitations of claim 26, the claimed method including the features that correspond to subject matter mentioned above in the rejection of claim 2 is applicable hereto.

Claims 33 – 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tabatabaei (US Patent 6,784,740) in view of Chen et al (US Patent 6,691,203).

Regarding claim 33, Tabatabaei is cited as explained in the above paragraph in the rejection of claim 1. Tabatabaei does not expressly teach the use of RISC. Such use of RISC is well known in the art (see Chen et al column 6, lines 5 – 15). Therefore it would be obvious to an ordinary skilled in the art at the time the invention was made to RISC with the system described above. The motivation or suggestion to do so is to further simplify the system.

Regarding claim 34, which inherits the limitations of claim 33,Tabatabaei in view of Chen et al does not expressly teach the output having an unbalanced duty cycle. At the time the invention was made, it would have been obvious to a person if ordinary skilled in the art to have system provide an output signal having an unbalanced duty cycle. Applicant has not disclosed that providing an output signal having an unbalanced duty cycle provides an advantage, is used for a particular purpose, or solves a stated problem. Therefore it would have been obvious to one of ordinary skilled in the art to modify Tabatabaei in view of Chen to obtain the invention as specified in claim 34.

Regarding claim 35, which inherits the limitations of claim 33, Tabatabaei further teaches providing a single ended signal (see figure 3).

Allowable Subject Matter

Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

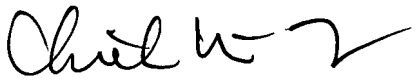
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jaison Joseph whose telephone number is (571) 272-6041. The examiner can normally be reached on M-F 9:30 - 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jaison Joseph
05/08/2007



CHIEH M. FAN
SUPERVISORY PATENT EXAMINER